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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/783,216	02/20/2004	Tim Tuan	X-1462-1P US	6678

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EXAMINER
LAM, NELSON C

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/22/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,216	TUAN ET AL.	
	Examiner	Art Unit	
	Nelson Lam	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *02/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication of 02/20/2004. Application 10/783,216 has been examined. In the examination of 10/783,216, claims 1-19 are pending.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. **Claims 1-5 and 7-11 are rejected under 35 U.S.C. 102(b)** as being anticipated by Jain (US Patent No. 6,038,386).

As per **claim 1**, Jain discloses a method of operating a programmable logic device comprising:

performing a timing analysis of a design of the programmable logic device (Abstract; col. 8, line 44-48; Fig. 8; col. 11, line 65 to col. 12, line 12);

determining timing slacks for active blocks of the design (Fig. 8, #810; col. 2, line 55-66);

assigning a first supply voltage to operate a first set of one or more active blocks of the programmable logic device (col. 3, line 61-67; Fig. 5; col. 8, line 63-66); and

assigning a second supply voltage, less than the first supply voltage, to operate a second set of one or more active blocks of the programmable logic device, wherein timing slacks of the first set of one or more active blocks are less than timing slacks of

the second set of one or more active blocks (col. 2, line 11-26; Fig. 2B; col. 4, line 57-58; col. 5, line 61-64; col. 9, line 39-54).

As per **claim 2**, Jain discloses the method of Claim 1, wherein the steps of assigning the first supply voltage and assigning the second supply voltage are performed in response to configuration data values stored during configuration of the programmable logic device (col. 2, line 48-66; Fig. 2E; col. 6, line 29-35).

As per **claim 3**, Jain discloses the method of Claim 1, wherein the steps of assigning the first supply voltage and assigning the second supply voltage are performed in response to user controlled signals provided during run time of the programmable logic device (col. 16, line 9-21).

As per **claim 4**, Jain discloses the method of Claim 3, further comprising generating the user controlled signals in response to operating conditions of the programmable logic device during run time (col. 16, line 9-21).

As per **claim 5**, Jain discloses the method of Claim 1, wherein the steps of assigning the first supply voltage and assigning the second supply voltage are performed in response to configuration data values stored during run time of the programmable logic device (Fig. 2D; Fig. 2E; col. 5, line 61-67; col. 6, line 17-22).

As per **claim 7**, Jain discloses the method of Claim 1, further comprising:

identifying the first set of one or more active blocks as active blocks in the design having timing slacks less than a threshold timing slack (col. 16, line 9-54); and

identifying the second set of one or more active blocks as active blocks in the design having timing slacks greater than the threshold timing slack (col. 16, line 9-54).

As per **claim 8**, Jain discloses the method of Claim 1, further comprising generating a configuration bit stream in response to the steps of assigning the first supply voltage and assigning the second supply voltage (Fig. 2D; col. 5, line 61 to col. 6, line 5; Fig. 2E; col. 6, line 17-35).

As per **claim 9**, Jain discloses the method of Claim 8, further comprising, configuring the programmable logic device in response to the configuration bit stream (col. 6, line 17-18; col. 6, line 29-35).

As per **claim 10**, Jain discloses the method of Claim 1, further comprising selecting the first set of one or more active blocks and the second set of one or more active blocks in response to the step of determining timing slacks (Fig. 5; Fig. 6; col. 8, line 63 to col. 9, line 29; col. 9, line 39-54).

As per **claim 11**, Jain discloses the method of Claim 1, further comprising selecting the second voltage supply to be a minimum voltage required to maintain functionality of the second set of one or more active blocks (Fig. 6; col. 9, line 39-44).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 6 and 12-14 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Jain in view of Mizuno et al. (US Patent No. US2004/0145955 A1). Jain discloses a method for controlling power consumption in a semiconductor integrated circuit.

However, Jain does not disclose the use of a third voltage source. Mizuno also discloses a method for controlling power consumption in a semiconductor integrated circuit that includes the use of a third voltage that Jain does not discloses. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the use of a third voltage source in the method of Mizuno in the method of Jain because this would improve Jain's invention since a third voltage source aids in optimization of a circuit block (Jain: col. 11, line 55-59).

As per **claim 6**, Jain in view of Mizuno discloses the method of Claim 1, further comprising assigning a third supply voltage, less than the second supply voltage (Mizuno: Abstract; [0016]), to operate a third set of one or more active blocks of the programmable logic device, wherein timing slacks of the third set of one or more active blocks are greater than timing slacks of the first and second sets of one or more active blocks (Jain: col. 2, line 11-36) (Mizuno: [0012]).

As per **claim 12**, Jain in view of Mizuno discloses a programmable logic device comprising:

a voltage supply terminal configured to receive a supply voltage (Mizuno: Fig. 1, #101; [0055]);

a plurality of programmable logic blocks, each having an associated timing slack (Jain: Fig. 1, #200; Fig. 2A; col. 4, line 19-58; col. 3, line 61 to col. 4, line 6);

a plurality of variable voltage regulators, each coupled between the voltage supply terminal and a corresponding one of the programmable logic blocks (Mizuno: [0008]; Fig. 24-26; [0117]; [0118]; [0119]); and

means for controlling the variable voltage regulators such that each of the variable voltage regulators provides an operating voltage to the corresponding one of the programmable logic blocks, wherein the operating voltage is selected in response to the timing slack associated with the programmable logic block (Jain: Fig. 10, #1010, #1080; col. 16, line 56-64; col. 18, line 38-67).

As per **claim 13**, Jain in view of Mizuno discloses the programmable logic device of Claim 12, wherein the means for controlling comprises one or more configuration memory cells coupled to each of the variable voltage regulators (Mizuno: [0007]; [0008]; [0009]; [0012]).

As per **claim 14**, Jain in view of Mizuno discloses the programmable logic device of Claim 12, wherein the means for controlling comprises one or more user input terminals coupled to each variable voltage regulator (Jain: col. 3, line 61 to col. 4, line 6) (Mizuno: [0007]; [0008]; [0009]; [0012]).

6. **Claims 15-19 are rejected under 35 U.S.C. 103(a)** as being unpatentable over Jain in view of Mizuno and further in view of Almulla (US Patent No. 5,612,892). Jain in view of Mizuno discloses a method of supplying voltage to circuit blocks. However, Jain in view of Mizuno does not teach the use of switches in supplying voltages. Almulla also discloses a method of supplying voltages to circuit blocks that includes the use of switches that Jain in view of Mizuno does not disclose. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the use of switches in the method of Almulla in the method of Jain in view of Mizuno since this would increase the speed of a signal path (Almulla: col. 3, line 41-44).

As per **claim 15**, Jain in view of Mizuno and further in view of Almulla discloses the programmable logic device of Claim 12, further comprising a plurality of level shifters coupled among the plurality of programmable logic blocks (Almulla: col. 3, line 36-51).

As per **claim 16**, Jain in view of Mizuno and further in view of Almulla discloses a programmable logic device (Jain: Abstract; col. 1, line 7 to col. 2, line 43) comprising:

a first voltage supply terminal configured to receive a first supply voltage (Jain: col. 3, line 61-67; Fig. 5; col. 8, line 63-66);

a second voltage supply terminal configured to receive a second supply voltage, less than the first supply voltage (Jain: col. 2, line 11-26; Fig. 2B; col. 4, line 57-58; col. 5, line 61-64; col. 9, line 39-54);

a plurality of programmable logic blocks, each having an associated timing slack (Jain: Fig. 1, #200; Fig. 2A; col. 4, line 19-58; col. 3, line 61 to col. 4, line 6);

a plurality of first voltage switches, each coupled between the first voltage supply terminal and a corresponding one of the programmable logic blocks (Almulla: col. 2, line 20-24; col. 3, line 29-36; Fig. 2, #225; col. 4, line 24-34).

a plurality of second voltage switches, each coupled between the second voltage supply terminal and a corresponding one of the programmable logic blocks (Almulla: col. 2, line 20-24; col. 3, line 29-36; Fig. 2, #225; col. 4, line 24-34); and

means for controlling the first and second voltage switches such that each of the programmable logic blocks having an associated timing slack less than a threshold timing slack is coupled to receive the first supply voltage, and each of the

programmable logic blocks having an associated timing slack greater than the threshold timing slack is coupled to receive the second supply voltage (Almulla: col. 2, line 20-24; col. 3, line 29-36; Fig. 2, #225; col. 4, line 24-34).

As per **claim 17**, Jain in view of Mizuno and further in view of Amulla discloses the programmable logic device of Claim 16, wherein the means for controlling comprises one or more configuration memory cells coupled to the first and second voltage switches. (col. 2, line 20-24; col. 3, line 29-36; Fig. 2, #225; col. 4, line 24-34).

As per **claim 18**, Jain in view of Mizuno and further in view of Almulla discloses the programmable logic device of Claim 16, wherein the means for controlling comprises one or more user input terminals coupled to the first and second voltage switches (col. 2, line 20-24; col. 3, line 29-36; Fig. 2, #225; col. 4, line 24-34).

As per **claim 19**, Jain in view of Mizuno and further in view of Alumlla discloses the programmable logic device of Claim 16, further comprising a plurality of level shifters coupled among the plurality of programmable logic blocks (Almulla: col. 3, line 36-51).

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nelson Lam whose telephone number is 571 272-8318. The examiner can normally be reached on Monday-Friday at 9am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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